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Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2014
(2008 Scheme)
Branch : Computer Science and Engg.
08.605 : HIGH PERFORMANCE MICROPROCESSORS

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks **each**.

1. What is branch prediction ? How does it improve the speed of execution of a processor ?
2. Why is the program memory of 8051 built using EPROM rather than RAM ?
3. Differentiate between paging and segmentation.
4. How are global variables stored in RISC processors ?
5. How is the address of a particular ISR obtained in 80286 ?
6. Explain SETHI instruction of SPARC processors.
7. Why are hardware counters used when the same function can be implemented using software loops in microcontrollers ?
8. Draw and explain the ARM instruction format.
9. Differentiate between RL and RLC instruction of 8051.
10. Explain the purpose of the following registers: GDTR, LDTR, IDTR.

(10×4=40 Marks)

PART – B

Answer **one** question from **each** Module. **Each** question carries **20** marks.

11. a) Explain in general, the concept behind hyperthreading technology. **10**

    b) What is out of order execution ? How is it handled using register renaming and instruction scheduling ? **10**

OR

12. a) With the help of a figure explain how virtual address is mapped to physical address in 80386. 15

b) What is the role of TLB in paging ? 5

13. a) How can the graph colouring problem be mapped to the compiler domain for register optimization ? 10

b) What are the main characteristics of Reduced Instruction set architectures ? Explain with examples. 10

OR

14. a) What is pipelining ? Explain the various pipeline optimization methods with examples and figures. 20

15. a) Explain in detail the serial data transmission modes of 8051. 10

b) Draw and explain the X-Y matrix keyboard configuration. 10

OR

16. a) Explain how characters are transmitted using time delay and polling in 8051. 10

b) Describe the internal memory organisation of 8051. 10